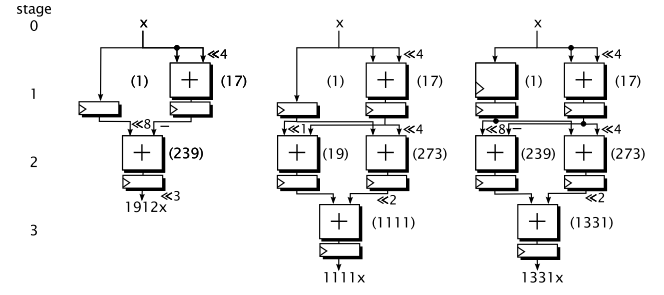
Reconfigurable Constant Multiplication for FPGAs

1. Contributions

This paper introduces a new heuristic algorithm to fuse multiple adder graphs into one graph used to build reconfigurable constant multiplier

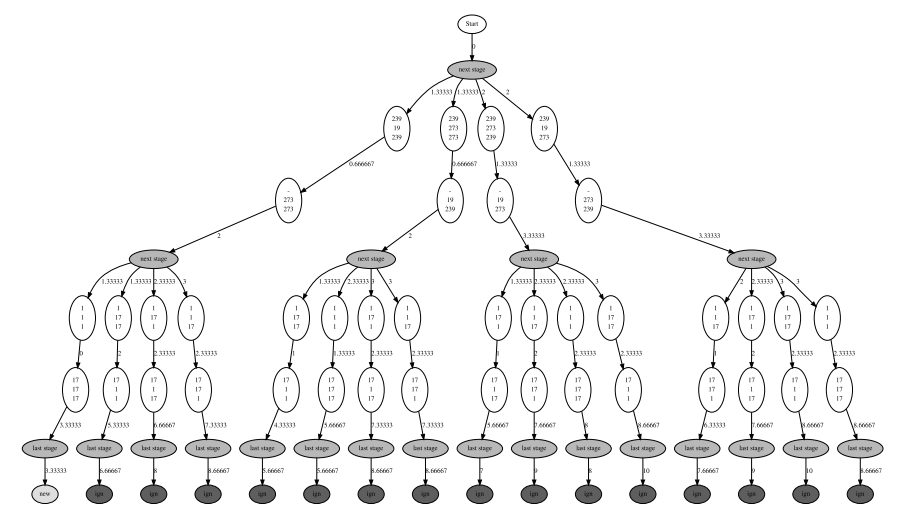
1. RPAG(reduced pipelined adder graph) solutions for single constant multiplication

The results of RPAG are adder graphs representing multiplier-less pipelined constant multipliers using additions, subtractions, and bit-shifts only. The main idea of multiplier-less multiplication as applied in RPAG is to compose a constant multiplication of an addition of shifted inputs.



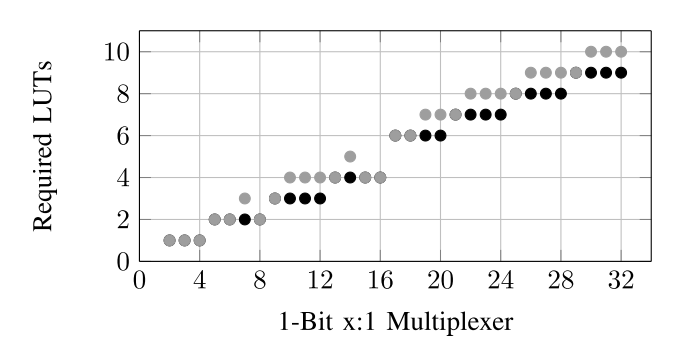
RPAG solutions for the constants 1912, 1111, and 1331

1. PAGs(pipelined adder graphs) fusion
   1. Purpose
      1. Minimal overhead overhead of possibly necessary multiplexers or switchable adder/subtractors(the multiplexers will be realized as a cascade of 2:1 multiplexers).
   2. Multiplexers can appear at the inputs of the successive stage in the following cases.
      1. Input has a different shift value.
      2. Input has a different source.
   3. The proposed fusion is backward-exploring, starting with the constant mapping of the output stage.
   4. Example



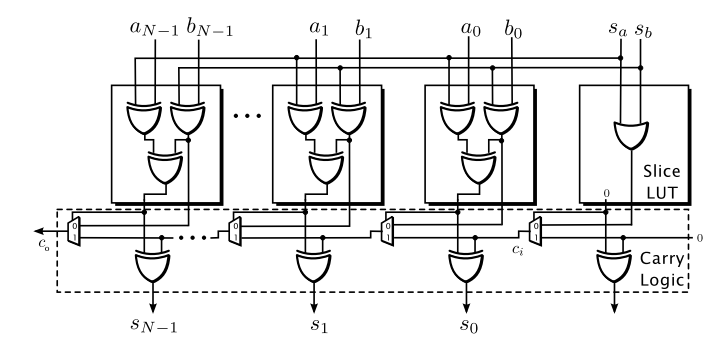
Full decision tree for the example with costs for each decision(1912, 1111, and 1331)

1. Low level optimization
   1. Multiplexer



Required LUTs for 1-Bit x:1 Multiplexer: ISE solutions(gray) vs Primitive usage(black)

* 1. Switchable Adder Subtractor Mapping



Realization of switchable adder/subtractor on Xilinx Virtex 5-7 slices

1. Results

